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2013 Nanotechnology 24 245303

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Nanotechnology **24** (2013) 245303 (9pp) doi:10.1088/0957-4484/24/24/245303

Fabrication of ultrahigh density metal–cell–metal crossbar memory devices with only two cycles of lithography and dry-etch procedures

B Y Zong[1,2], J Y Goh[2,3], Z B Guo[2,4], P Luo[2], C C Wang[2], J J Qiu[2], P Ho[2], Y J Chen[2], M S Zhang[2] and G C Han[2]

[1] Temasek Laboratories, National University of Singapore, #09-02, 5A Engineering Drive 1, 117411, Singapore
[2] Data Storage Institute, Agency for Science, Technology and Research (A*STAR), DSI Building, 5 Engineering Drive 1, 117608, Singapore
[3] National Junior College, 37 Hillcrest Road, 288913, Singapore
[4] Core Labs, King Abdullah University of Science and Technology (KAUST), Thuwal 23955-6900, Saudi Arabia

E-mail: tslzb@nus.edu.sg and baoyuzong@hotmail.com

Received 17 January 2013, in final form 19 April 2013
Published 20 May 2013
Online at stacks.iop.org/Nano/24/245303

Abstract

A novel approach to the fabrication of metal–cell–metal trilayer memory devices was demonstrated by using only two cycles of lithography and dry-etch procedures. The fabricated ultrahigh density crossbar devices can be scaled down to ≤70 nm in half-pitch without alignment issues. Depending on the different dry-etch mechanisms in transferring high and low density nanopatterns, suitable dry-etch angles and methods are studied for the transfer of high density nanopatterns. Some novel process methods have also been developed to eliminate the sidewall and other conversion obstacles for obtaining high density of uniform metallic nanopatterns. With these methods, ultrahigh density trilayer crossbar devices ($\sim 2 \times 10^{10}$ bit cm^{-2}-kilobit electronic memory), which are composed of built-in practical magnetoresistive nanocells, have been achieved. This scalable process that we have developed provides the relevant industries with a cheap means to commercially fabricate three-dimensional high density metal–cell–metal nanodevices.

(Some figures may appear in colour only in the online journal)

1. Introduction

Smaller miniature devices with higher capacities or more functions are the trend in the extremely competitive electronic products market, e.g. in hard disk drives, thumb drives, mobile phones, and the integrated circuit (IC) chip industries [1, 2]. To improve the capacity or function of the miniature devices, much higher density and finer nanopatterns are required. For example, to achieve a high capacity of more than 1 Tb in^{-2} memory, the pitch of the storage bits should be <30 nm [3]. The fabrication process of high density fine nanopatterns is critical in the production of miniature nanodevices [4]. Conventional resist lithography and dry-etch are usually used in the fabrication process. This process provides a cost-effective and feature-scalable preparation of nanostructures compared to other methods (e.g. self-alignment), and matches the different shape and size requirements of the nanodevices [5, 6]. Thus, this process is widely used in the production of commercial nanodevices nowadays [7]. To fabricate trilayer metal-electrode/magnetoresistive (MR) cell/metal-electrode memory devices, each layer (including the metallic nanocell layer) typically requires one cycle

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of lithography and dry-etch procedures [8]. With this common method, although devices with loosely distributed (usually half-pitch > 200 nm) sub-50 nm feature sizes can be readily achieved [2, 9], some critical problems arise from the fabrication of three-dimensional (3D) devices when the characteristic size (e.g. the dimension of electrode arrays) is reduced to less than ≤100 nm for the half-pitch. For instance, there are challenges to convert high density resist nanopatterns into smooth device nanostructures, and to define or locate accurately the fine practical cell nanopillars on these array-electrodes with a half-pitch of less than ≤100 nm, etc [10, 11]. Currently, an approach to the fabrication of trilayers for practical metal–cell–metal memory devices, with a half-pitch less than 100 nm, has not been reported, despite the increasing demand for the miniature 3D memory devices and their related manufacturing processes (e.g. the transfer of high density nanopatterns) from the relevant industries [12, 13]. Even though resist lift-off and other alternative methods, such as one-step deposition via selective etching of multilayer superlattice films [14, 15], or the embedding of nanowires in thin polymer slabs [16], have been employed to prepare thin bilayer metal crossbars (usually ≤10 nm in thickness for each layer) with an ultrahigh density of ≤100 nm in half-pitch [17], the subsequent fabrication of <100 nm practical fine metallic cells on each junction of crossbar circuits to form a commercial memory device remains a critical challenge [17, 18]. Thus, the search for a suitable method to fabricate high density multilayer 3D nanodevices, particularly a cost-effective simple way for industry, is of interest and in high demand.

Herein, by using a novel method via two cycles of lithography and dry-etch procedures as well as suitable etch methods during the nanopattern transfer, we demonstrated the successful fabrication of trilayer crossbar memory devices with a half-pitch of less than 70 nm through the conventional cost-effective processes. With the development of simple process skills to shorten the fabrication nanoprocess as well as to eliminate the transfer defects, practical ultrahigh density 3D metal-MR cell-metal crossbar nanodevices were achieved.

2. Experimental methods

In this investigation, a high resolution (≤2 nm) electron-beam nanolithography system (ELS-7000) was used to expose the high density resist nanopatterns. The resist and device nanopatterns were configured on SiO_2 isolator wafers. During the nanolithography process, the positive e-beam resist ZEP(520A) and negative hydrogen silsesquioxane (HSQ) were used. The metallic device films were sputter-deposited on the SiO_2 wafer using a thin-film sputter system (MPS-6301-SP). During the transfer of resist to device nanopatterns via dry-etching, a Microetch ion-beam system (IBE, RF-350) was used. The applied voltage for the IBE system was 250–400 V at a frequency of 50 Hz. The developers used were ZED-N50 (with ZMD as the rinsing solution) and tetramethylammonium hydroxide for ZEP and HSQ resists, respectively. Resist lift-off was carried out by immersing the sample in Remover PG solution in an ultrasonic bath for 20–30 min. The thickness and images of all nanopatterns were measured using an atomic force microscope (AFM, Dimension 3100) or a field emission scanning electron microscope (FESEM, JSM 7401F). The exposure energies of the resists and measurement methods for the nanopatterns and MR nanocells were similar to those reported previously [19, 20].

3. Results and discussion

The fabrication process for the trilayer metal-MR cell-metal crossbar memory devices was directly achieved from traditional scalable lithography and dry-etch processes via simple novel two-cycle procedures. The successful transfer of high density resist nanopatterns to uniform device nanoarrays was approached via a careful dry-etch by selecting suitable etch-angles.

Figure 1 illustrates a comparison between the common conventional method and our developed simple method for the preparation of a trilayer crossbar device. The common preparation method, a process with three cycles of lithography and dry-etch procedures, usually requires an additional cycle for the fabrication of nanocells compared to our novel simple method. For the fabrication of memory devices with high array density (e.g. ≤100 nm in half-pitch) by using the common method, the existing challenges include (i) locating recording cell elements on the fine <100 nm electrode nanoarrays, (ii) converting high density resist nanopatterns to smooth device nanostructures, and (iii) subsequently locating the fine high density top-electrode nanoarrays on the fine <100 nm nanocells.

3.1. Different conversion mechanisms for high and low density device nanofeatures

For the transfer of resist nanopatterns to high density or fine multilayer device nanostructures, ion-beam etch (IBE) was preferred since it used an inert Ar-gas source and produced a smaller difference in etch-rates for the different metallic layers. A better side profile was obtained for the converted device nanopatterns in comparison to other dry-etch methods [19, 21]. Based on the nanopattern transfer mechanism via IBE etching, the transfer of ultrahigh density nanopatterns was found to be quite different from that of loosely distributed nanopatterns during etching. Figures 2(a) and (b) show the comparison for dry-etching low and high density resist nanopatterns, respectively. In the dry-etch, a fluid etch medium with a stable energy and continuous contact with the etching position was required for a successful etch. When converting device nanofeatures from high density resist nanopatterns, the closely packed resist patterns hindered the effective penetration of the etch medium (namely ion-beam) into the trench bottoms. The issue arose due to the reduced ion-beam energy after the absorption or shading by the side or top surfaces of the high density resist nanopatterns. At the same time, the etched or reflected ion-beam residues could not disperse readily or quickly from the narrow patterned trenches. This situation prohibited the incident etching

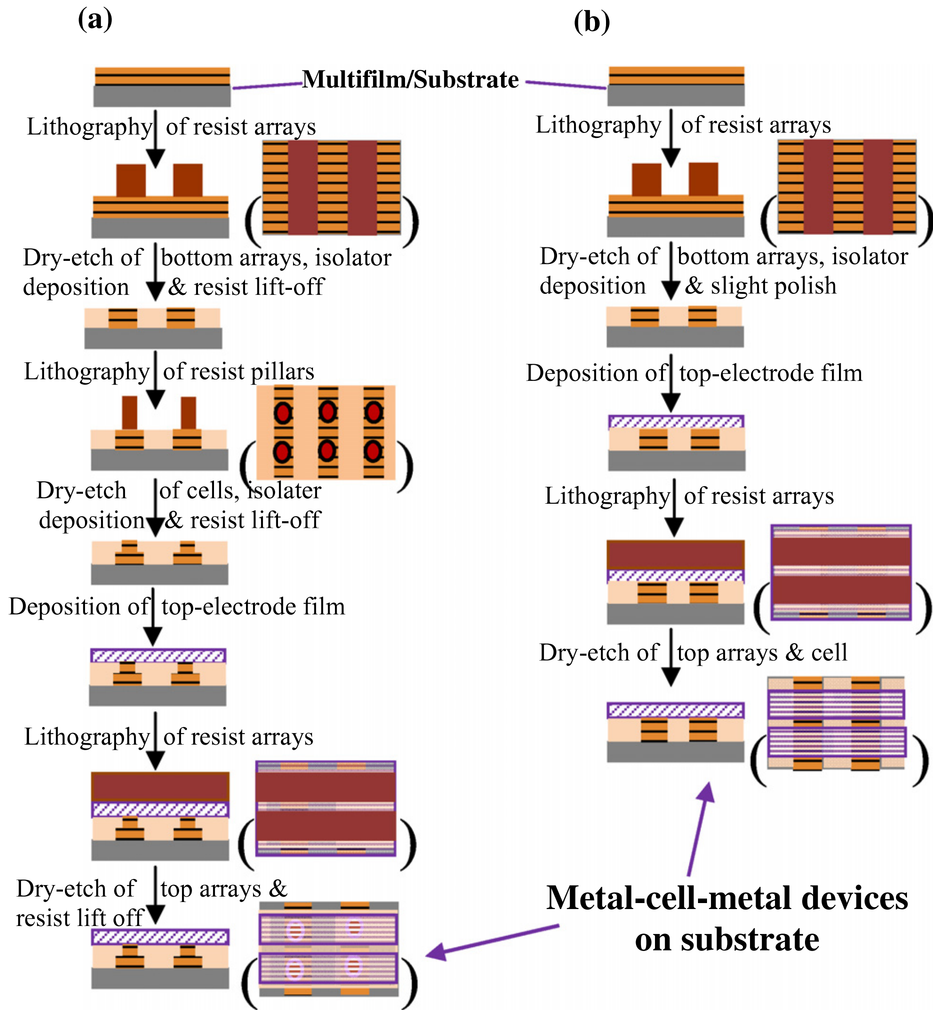

Figure 1. Schematic illustration of (a) the conventional method and (b) our new approach for the fabrication of trilayer nanodevices via three and two cycles of lithography and dry-etch processes, respectively. The pictures in brackets show the corresponding top views.

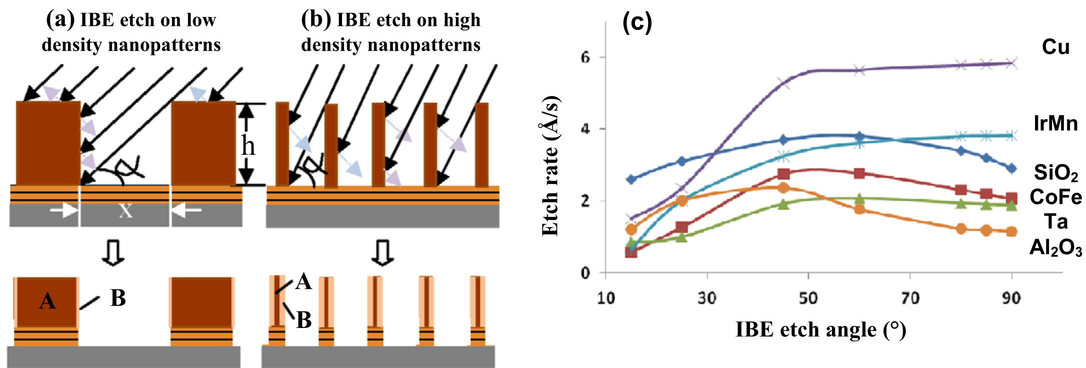

Figure 2. Comparison of dry-etching (a) low and (b) high density resist nanopatterns at the minimum etch angle of the ion-beam to the substrate. ‘A’ represents the remaining resist residue-patterns while ‘B’ represents the sidewalls attached on the resist residue-patterns after the dry-etch. (c) The etch-rates for commonly used bare films with different etch-angles. The etching voltage and current used were 250 V and 0.42 mA cm^{-2}, respectively.

medium from reaching the surfaces of the etching metal film (shown in figure 2(b)), which was located at the trench bottom of the resist nanopatterns, hence reducing the etch-rates of the device metal films. Moreover, the confined etching-residues could damage or re-deposit on the sides of the fine resist nanopatterns. The re-deposition enhanced sidewall defects of the converted device nanopatterns. After etching, the sidewall (B) depicted in figure 2(b) formed a significant portion of the fine resist residue-patterns, which almost entirely wrapped the fine device nanopatterns from two sides. This was quite different from the big and loosely distributed resist patterns (shown in figure 2(a)). The fine resist residue-patterns

wrapped by the sidewalls were more difficult to remove during the lift-off process due to the difficulty for lift-off solution to penetrate into the resist residues. Thus, during the conversion of high density nanopatterns, there were critical challenges in ensuring that the etch medium moved readily in and out of the resist pattern trenches without severely damaging the fine resist nanopattern-shapes during dry-etching and minimizing sidewall defects after the etch, etc. Most of such challenges were irrelevant during the etch of big sub-micron or loosely distributed fine nanopatterns, as the etch medium could readily approach or reflect away from the etching position without any obstacles for the loosely distributed fine nanopatterns. As such, there was a much lower portion of sidewalls for the big patterns. Thus, converted fine device nanofeatures (such as those down to sub-20 nm [2, 9]) are commonly reported, whereas reported instances of converted high density sub-50 nm device features have been few thus far. Our solutions to these challenges were based on these analyses of the etching natures and mechanisms.

3.2. Selection of suitable IBE dry-etch angle and energy

The sidewall defects after the dry-etch and resist lift-off were a major challenge in the common fabrication method (depicted in figure 1(a)), and the sidewall defects could exist in both high and low densities of transferred device nanopatterns, despite there being a better situation for the low density nanopatterns (as stated above). Figure 3(a) shows the sidewall defects, which are still significant although they were partially wiped out with residue-free cloths. To reduce sidewall defects and achieve device nanopatterns with a good profile during IBE etching, the dry-etch angle of the ion-beam to the sample surface was critical. A suitable etch angle could prevent the ion-beam (etch medium) and the reflected residue ion-beam from being fully shaded and confined by the resist nanopatterns. Figure 2(c) also illustrates the etch-rates for commonly used materials with respect to the different etch-angles. Table 1 shows the relationship between the minimum (min.) etch angle to the substrate surface and the gap or height of the resist nanopatterns. To obtain high contrast device nanopatterns with lower sidewall height, an etch angle smaller than 90° was favourable. Experimental results showed that there were almost no sidewall defects by using an etch angle slightly larger than 45° for the loosely distributed resist patterns, if there were no shading and confining for the ion-beam. However, with increase in nanopattern density (namely a decrease of the nanopattern gap), the range of dry-etch angles, with respect to the different heights of resist nanopatterns, became much narrower when considering the shading and reflection of the ion-beam (depicted in figure 2). For example, table 1 illustrates that for resist nanopatterns with a 5 or 50 nm gap and a corresponding height from 100 to 25 nm, the minimum etch angle was between 87°–79° and 63°–27°, respectively. It is noted that 90° was the maximum etch angle, where the etching ion-beam was normal to the sample surface. Thus, an optimized dry-etch angle should be used in the nanopattern transfer after further consideration of the device profile, sidewall issue, shading

Table 1. Relationship between the minimum IBE etch angle and the height or gap of the resist nanopattern.

Min. etch angle, α (deg)	Height of resist nanopatterns, h (nm)	Gap of resist nanopatterns, x (nm)
87	100	
86	75	5
84	50	
79	25	
84	100	
82	75	10
79	50	
68	25	
76	100	
72	75	25
63	50	
45	25	
63	100	
56	75	50
45	50	
27	25	
53	100	
45	75	75
34	50	
18	25	
45	100	
37	75	100
27	50	
14	25	

and confining of the ion-beam, and the slight change in etch-rate for the different etch-angles. During the conversion of high density round resist pillars to device nanocells by using IBE etch, the substrates could be continuously rotated to achieve a good cell profile, as the reflected ion-beam was not confined within the trenches of the high density of resist pillars. However, when converting high density nanoarrays of bottom- or top electrodes on a rotating substrate during the dry-etch, the reflected ion-beam, readily confined within the trenches of the resist arrays, would damage the fine resist patterns at the high energy, as depicted in figure 3(b_i) (top-left image). The top-right image in figure 3(b_{ii}) shows the original fine resist nanopatterns before etching. In this situation, to prevent the fine resist nanopatterns from damage, it was ascertained that the etching incident and reflected beams in the planar surface had to be parallel to the resist array direction for the effective etching of array bars. This prevented the confinement of the reflected residue beam within the dense resist nanopatterns. During the dry-etch of high density resist nanopatterns, the shading and absorption of the ion-beam energy by the top and side surfaces of the resist patterns were more significant in terms of unit substrate area as compared to the loosely distributed nanopatterns. Thus, a higher etching energy (e.g. ion-beam voltage $\geq$ 230 V) was required. Furthermore, when etching device films of the same thickness, a longer time was required for the high density resist nanopatterns. As such, for the same dry-etch time, the etching depth of the device film on one sample

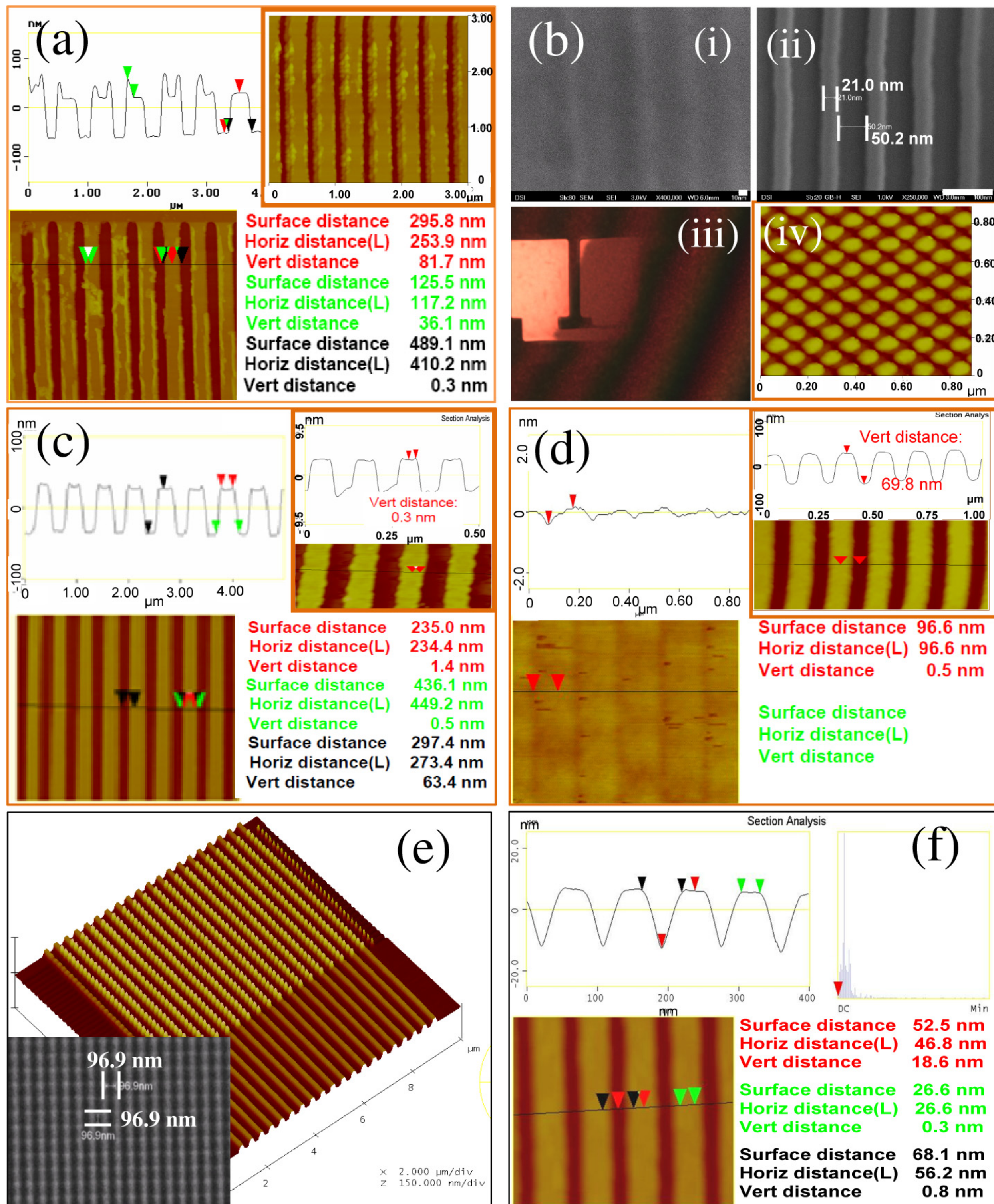

Figure 3. (a) AFM image of sidewall defects from the common dry-etch and resist lift-off method while the 3 μm × 3 μm inset shows the device nanopatterns with treated sidewalls using O_2 plasma. (b_i) and (b_{ii}): FESEM images of the completely damaged (after dry-etching) and the original high density ZEP nanopatterns, respectively. IBE was carried out with the common sample-rotating method; (b_{iii}): 0.3 mm × 0.3 mm optical image showing an uneven CMP polished portion of a 4″ wafer while removing the sidewalls; (b_{iv}): 1 μm × 1 μm AFM image of Co/Pt/Co pillars after dry-etching without resist lift-off. The scale bars of (b_i) and (b_{ii}) are 10 nm and 100 nm, respectively. (c) and its inset: AFM images of the converted device nanopatterns of different densities with a ∼5 nm Au film to wrap the ZEP resist nanopatterns for eliminating the sidewalls. The horizontal axis intervals in the left and right images are 1 and 0.25 μm, respectively. (d) AFM image of the converted device nanoarrays, where the gaps were filled with HSQ resist. The inset depicts the dry-etched nanoarrays before the HSQ filling. The horizontal axis intervals in the left and right images are 0.20 and 0.25 μm, respectively. (e) Transferred ∼100 nm metallic nanocells from resist nanopillars on crossbar circuits. The inset shows the ∼60 nm nanocells on cross-points dry-etched from the crossed resist arrays. (f) AFM image of the slightly lapped device arrays, which were converted from the almost fully dry-etch of the resist nanoarrays.

surface varied with the different density resist nanopatterns. The etching depth in the high density resist nanopatterns was much shallower than that in the loosely distributed resist nanopatterns or bare films. For instance, when etching pure Ta film, on which different density resist nanopatterns were lithographed, for 150 s with beam voltage of 350 V and power 0.5 mA cm^{-2} at an etch angle of 86°, the etched Ta depth was 46, 42, 35, and 16 nm among resist nanoarrays with a half-pitch of 415, 160, 120, and 78 nm, respectively.

3.3. Tackling the defects in nanopattern transfer

Sidewall defects, the complex products of re-deposited metal films and burnt/over-cured (aged) resists caused by the high energy dry-etching, could also result in difficult resist lift-off (as mentioned above) after the etch-transfer of the resist nanopatterns to device nanostructures. They could not be dissolved in solvents and other solutions or fully removed by plasma treatment. The inset (top-right corner) of figure 3(a) shows the remnant sidewalls after O_2 plasma treatment for 60 s (at 100 W and a gas flow-rate of 50 sccm), for the nanopatterns in figure 3(a). Accordingly, the sidewalls were difficult to lift off by the usual means of cleaning. Some sidewalls could be removed through the deposition of SiO_2 or Al_2O_3 into the gaps of the device nanopatterns after the dry-etch, followed by resist lift-off and chemical mechanical planarization (CMP polishing). However, it was hard to achieve a good profile of nanopatterns on the whole wafer surface for the higher sidewalls (usually $\geq$ the height of the device nanopatterns). After polishing, some sidewalls remained high at some parts of the wafer surface while the sidewalls including device nanopatterns at other parts were polished away (shown in the bottom-left image in figure 3(b_{iii})). A contributing factor was the limitation of CMP machines, which usually have a $\geq$8% tolerance error in polishing uniformity on a wafer (e.g. $\geq$4″) surface [22]. The difficulty in the resist lift-off was also found when the thickness of the resist nanopatterns was left at less than a certain value after the etch by a high energy ion-beam, due to the over-cured or burnt fine resist nanopatterns. Hence, in order to minimize the difficulty in resist lift-off, higher resist nanopatterns (namely larger aspect ratio) were required using the common transfer method via dry-etch and lift-off procedures. This posed a process difficulty for the device fabrication, as it was hard to achieve a high aspect ratio of $\leq$70 nm resist nanopatterns, with normal commercial electron-beam resists, by using a conventional method in the lithography process [20, 23]. As such, the sidewall defects and difficult lift-off issues were critical obstacles in the conversion of device nanopatterns [23]. This is one major reason why there has been limited progress reported so far on practical high density crossbar memory devices with half-pitch of $\leq$100 nm. To overcome the sidewall issues after the nanopattern transfer, a few alternative methods to replace CMP polishing have been reported. For instance, a thin layer of Al or Al_2O_3 film, as an alkaline-soluble interim layer between the device nanofilm and resist nanopatterns, is reported to be able to eliminate the sidewall defects [24]. After the transfer of nanopatterns, this Al-based film is etched away in an alkaline solution together with the attached resist residue and sidewalls. However, such an approach was shown to be only suitable for the device films that possessed high tolerance to alkaline solutions. It was unsuitable for multilayer device films containing layers susceptible to alkaline etchants, for example Al, Mg, Zn, Sn, IrMn, Al_2O_3, ZnO, etc. These layers would be etched away together with the interim Al film by the alkaline solution. To solve this issue, we developed other novel simple methods, which readily eliminated the sidewall problems. For example, deposition of a thin 4–8 nm metal film (e.g. Au, Cr, Ta), by using an e-beam evaporator or low-energy sputtering, before the resist coating and immediately after the formation of resist nanopatterns on the device film via developing, was one means. After the deposition, the thin metal film wrapped the fine resist nanopatterns (any type of e-beam resist) before dry-etching. Figures 3(c) and (a) show the comparison of the etched 250–275 nm CoFeB/Al_2O_3/CoFe nanopatterns, which were transferred from ZEP resist nanopatterns with and without 4–8 nm Au evaporated before IBE dry-etching, respectively. After IBE dry-etching and resist lift-off, it is clear that the sidewalls are prevalent for the magnetic nanopatterns (shown in figure 1(a)) converted from the resist patterns without Au coating. On the contrary, when the resist patterns were wrapped by a thin layer of gold, the converted magnetic nanopatterns were smooth without sidewall defects (depicted in figure 3(c)). This is because the thin conductive gold film could prevent the resist from being burnt during dry-etching by quickly dissipating the IBE-induced charge and heat. This allowed the resist pattern-residues to readily dissolve in the lift-off solution. Furthermore, when the thin film was etched into small device structures, the thin metal film located between the device film and resist residue-patterns could be easily removed under ultrasonic vibration in solvent during the lift-off process after the dry-etch, since the adhesion of the thin metal film to the device film was weak due to the low-energy deposition, but strong enough to prevent the developer solution (without ultrasonic vibration) from peeling the whole sheet film on the device film surface in the developing of the resist nanopatterns. The inset of figure 3(c) shows the higher density Co/Pt/Co/Pt nanopatterns (with a half-pitch of ∼63 nm) converted using this method.

The sidewall issue could also be mitigated by using curable e-beam resists (e.g. HSQ, Al, and Mg based resists), which could be converted to an isolator layer after curing [25]. By using dry-etch transfer, the sidewall defects were found to emerge only after lifting-off the resist pattern-residues. After the dry-etch and before the resist lift-off, there were no sidewalls exposed as the sidewall metal film was attached to the sides of the resist patterns. The bottom-right image in figure 3(b_{iv}) shows such dry-etched ∼40 nm Co/Pt/Co pillars with negligible sidewalls. For multilayer device nanopatterns (such as crossbar circuits, where a 5–30 nm thick isolator layer was usually used to separate the layers), after the transfer of the first layer, the sidewall films could be buried by coating the curable resist again without lifting-off the remaining curable resist nanopatterns after the dry-etch. Hence no sidewall

defects were present. In addition, the sidewall metal film attached to the sides of the resist patterns was always lower than the surface of resist nanopatterns by using a dry-etch angle smaller than 90°. Thus, there was no short-circuiting issue after coating the curable resist. The coated resist not only acted as the isolator layer after being cured, but also wrapped the sidewall metal and smoothed the device surface by filling the surface pits and gaps among the nanopatterns (even for larger pitch nanopatterns) after dry-etching. Figure 3(d) shows 80 nm nanoarrays in a larger half-pitch of ∼85 nm with the gaps being filled with 85 nm cured HSQ resists, while the inset in the figure (top right) shows the nanopatterns before the resist coating. In addition, the thickness of the coated resist could be adjusted by changing the spin-coating speed or the resist concentration according to the process requirement. After the coating, the second device layer could be readily fabricated on the first layer without being affected by the sidewall defects. By using this method, the sidewall defects were not only readily eliminated, the fabrication process was also shortened by abandoning the lift-off procedure for the resist residues after dry-etching. As a result, tri- or multilayer devices could be easily piled up. For instance, figure 3(e) depicts ∼100 nm uniform dry-etched metallic nanocells (with some resist residues on them) built on crossbar circuits with a half-pitch of 100 nm × 200 nm. From a physical geometry point of view, the membrane devices constructed with multilayer crossbar-memories can achieve the highest data storage density in unit volume.

Further investigation results revealed that the sidewall and difficult lift-off issues could also be simply prevented by fully or almost fully converting uniform resist nanopatterns into device nanopatterns with an accurately calibrated etch-rate. As such, resist nanopatterns and sidewalls would almost be fully etched away during the pattern transfer, which resulted in the absence of sidewall defects and eliminated the procedure of resist lift-off. Moreover, as in the previous method, relatively high quality, uniform, and smooth surface device nanopatterns could be achieved due to the removal of the lift-off process and transfer defects. The inset image of figure 3(e) shows the fine ∼45 nm × 45 nm cells being directly converted by fully etching crossbar HSQ nanopatterns until the surface of the cell film. For this method, the required height of the resist nanopatterns could also be lower (without requiring high aspect ratio resist nanopatterns sometimes) in comparison to that used in the common conversion method via the dry-etch and lift-off procedures. As no sidewall defects were present, the uniformity of lapping or CMP polishing for the removal of the residues on the whole wafer surface after the dry-etch could be greatly improved. Thus, this method was effective in achieving smooth and uniform surfaces of device nanopatterns on a large area. Figure 3(f) shows an example of the converted device nanoarrays after almost fully dry-etching the resist nanopatterns, and subsequently slight lapping of the device surface to fully remove the resist residues.

3.4. Fabrication of trilayer 3D devices

By using only two cycles of lithography and dry-etch processes to fabricate 3D trilayer devices, with reference to the schematic illustration in figure 1(b), the bottom arrays containing cell and bottom electrode films could firstly be converted from sub-100 nm resist arrays via dry-etching. The conversion proceeded either by fully etching the resist arrays or half-etching and lifting-off high aspect ratio resist nanopatterns wrapped by a 4–8 nm metal film (figure 4(a), from our modified HSQ resist [19]). For the fully dry-etch of resist patterns, the top surfaces of the device arrays (depicted in figure 4(b)) were slightly lapped out subsequently after coating a thin (10–25 nm) SiO_2, Al_2O_3 isolator or curable HSQ resist layer (to separate the bottom and upper array circuits). A top-electrode film (20–30 nm) was then sputtered on the clean bottom device arrays and whole wafer surface. Subsequently, another cross-layer of resist array patterns was lithographed on the top-electrode film. The top electrodes and nanocells could be converted from the resist arrays by etching the metallic multilayer device film. The etching was through the layers of top-electrode and cell films till the bottom electrode surface (for retaining bottom electrodes). As the cell films were etched together with the top electrodes, the nanocells were formed between two layers of electrode arrays. The cross-points of the two-layer arrays determined the cell shapes. Our experimental results critically revealed that with the use of these novel cross-nanoarrays to define the fine <100 nm cell and top-electrode arrays, the positions of the fine nanocell and top-electrode nanoarrays (shown in the inset of figure 4(c)) could be readily and accurately aligned on the high density of fine metallic bottom nanoarray-electrodes, with a half-pitch down to ≤ 70 nm, without any failure. With these novel procedures, practical fine nanocells (with multilayer films) were readily fabricated between the high density metallic nanoarrays or crossbar nanocircuits. Once the device was converted, a thin layer of isolator could be deposited to protect the surface of the device. As such, the complete high density trilayer 3D memory device core wrapping practical fine MR nanocells at each cross point, as depicted in figure 4(c) and its inset, was fabricated from the two cycles of lithography and dry-etch procedures. The device in figure 4(c) and the inset was composed of two layers of Ta (20 nm) crossbar circuits and embedded magnetic tunnel junction (MTJ) cells (one type of MR cells) of ∼65 nm at each cross point. A 25 nm Al_2O_3 layer was used to separate the crossbar circuits with a half-pitch of ∼70 nm. The layer structure of the nanocells included a free layer (CoFeB 2)/tunnelling barrier layer (MgO 1)/reference layer (CoFeB 5)/space layer (Ru 0.8)/pinned layer (CoFe 3.5)/antiferromagnetic layer (IrMn 8), where all digital numbers are the thicknesses for each layer in units of nanometres. As the magnetization direction of the CoFeB reference layer was fixed by the CoFeB pinned layer through exchange-coupling, a small external magnetic field, applied in the film plane, could change the magnetization direction of the CoFeB free layer away from that of the reference layer. When the magnetization directions in the free and reference layers were parallel, a low resistance state (R_{min}, ‘0’ state) could be obtained, e.g. ∼21 kΩ for one MTJ cell in this device (depicted in figure 4(d)). In contrast, when the magnetization directions were antiparallel, a high resistance

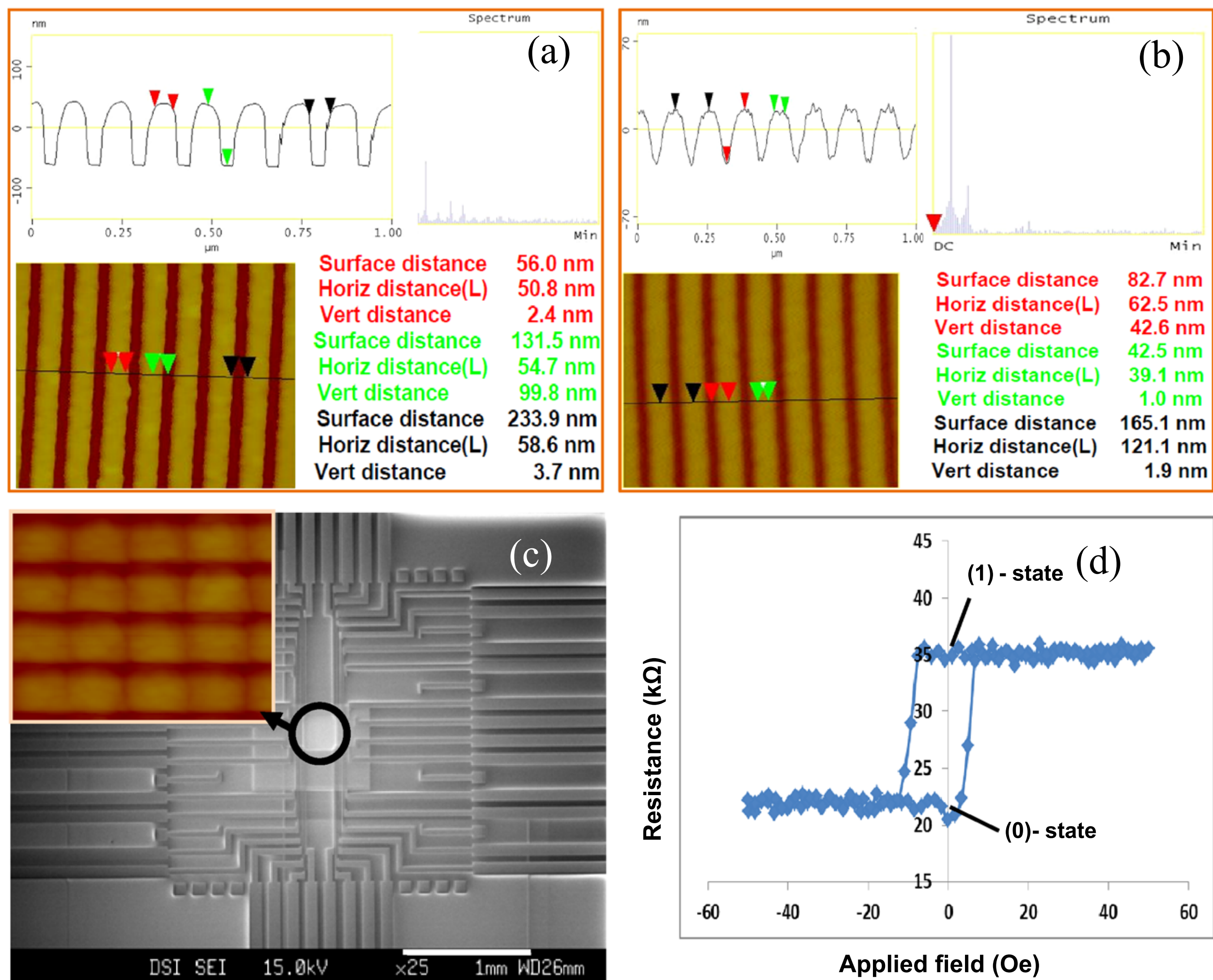

Figure 4. (a) AFM image of high aspect ratio HSQ resist nanoarrays (doped ~3 nm PtFe nanoparticles) lithographed on top-electrode film and wrapped by ~6 nm Au films. (b) AFM image of multifilm device arrays converted from fully etching resist nanoarrays. During dry-etching, the ion-beam was parallel to the array direction. (c) FESEM image of a trilayer device wrapping ~70 nm × 75 nm MTJ nanocells at the cross-points (shown in the 0.5 μm × 0.5 μm inset) by using the two cycles of lithography and dry-etch procedures. The scale bars in (c) are 1 mm. (d) MR curve of a MTJ nanocell.

state (R_{max}, '1' state) (e.g. ~35 kΩ for the cell) was obtained. The magnetoresistance ratio (namely the on/off ratio) was defined by $MR\% = (R_{max} - R_{min})/R_{min}$, which is about 66% for the memory device shown in figure 4(d). To the best of our knowledge, the fabrication of such a high density of practical memory devices is the first of its kind although it is highly sought after in the data-storage industry.

Further experimental results showed that the crossbar devices, from the simple two cycles of lithography and dry-etch procedures, had the advantage of low contact resistance at the interface between nanocells and top electrodes. This is because there was a larger and cleaner contact area at the interface as compared to the pit point contact of common pillar cells from the common three cycle transfer method. This scalable manufacturing method was also evaluated and used for the preparation of devices of low density with any mono- or multifilm-structural cells. It could also be used for devices with different sizes, thicknesses, and materials (such as semiconductors), since it was relatively easy to convert nanostructures of semiconductors (e.g. Si) and non-metallic materials (e.g. AsN and SiN, used in resistive random access memory (ReRAM) devices) of different densities (particularly in single or a few layers) from the resist nanopatterns via dry-etching. This is the result of the higher dry etch-rates [24] of semiconductors and non-metallic materials compared to the metal and oxide materials used in this work. Therefore, this simple fabrication method could be used for the preparation of various types of multilayer 3D nanodevices (e.g. ReRAM, magnetoresistive random access memory (MRAM), spintronics and memristor devices), and would be of great potential for nanodevice industries and technologies.

4. Conclusions

In summary, a simple novel manufacturing method to shorten the fabrication process was developed to achieve ultrahigh density of practical 3D crossbar nanodevices.

Through suitable dry-etch angles and energies, as well as developed pattern-transfer methods, the challenges faced in the transfer of high density nanopatterns and the preparation of trilayer nanodevices has been overcome. The methodology has produced 3D crossbar devices with practical metallic nanocells with a new fine scale of $\leq$70 nm in half-pitch. This fabrication strategy presents a general, cost-effective way to fabricate tri- or multilayer metal–cell–metal memory nanodevices, and is possibly capable of catering for density improvements in both horizontal and vertical directions to meet the demands of future data storage and integrated circuit maps [26, 27].

Acknowledgment

The authors thank Mr S H Soh for his practical support during this work.

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